Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.An erasable programmable read only memory comprising:

two serially connected P-type metal-oxide semiconductor (MOS) transistors,wherein a first P-type MOS transistor acts as selecttransistor, a gate of said first P-type MOS transistor is coupled to select gate voltage, a first node of said firstP-type MOS transistor is connected to source linevoltage, a second node of said first P-type MOS transistor is connected to a first node of a second P-type MOS transistor, wherein a second node of said second P-type MOS transistor is connected to bit line voltage,

wherein a gate of said secondP-type MOS transistor serves as a floating gate, wherein said erasable programmable read only memory does not need to bias a certain voltage on a control gate for programming and thereby injecting hot carriers onto said floating gate, and wherein said erasable programmable read only memory is capped by dielectric materials which are transparent to ultraviolet (UV) light.

[c2] 2.The erasable programmable read only memory of claim 1 wherein during an erase mode, carriers stored in said floating gate are removed by exposing to UV light and said UV light irradiates said floating gate through said dielectric materials capped on said erasable programmable read only memory.

[c3] 3.The erasable programmable read only memory of claim 2wherein said dielectric materials comprise silicon oxynitride.

[c4] 4.The erasable programmable read only memory of claim 2wherein said dielectric materials comprise silicon dioxide.

[c5] 5.The erasable programmable read only memory of claim 2wherein said dielectric materials comprise any material that is UV-transparent.

[c6] 6.An erasable programmable read only memory comprising:
two serially connected P-type metal-oxide semiconductor (MOS) transistors,wherein a first P-type MOS transistor acts as selecttransistor, a gate of said first P-type MOS transistor is electrically coupled to select gate voltage, a first node of said first P-type MOS transistor is connected to source line voltage, a second node of said

first P-type MOS transistor is connected to a first node of a second P-type MOS transistor,
wherein a second node of said second P-type MOS transistor is connected to bit line voltage, wherein a gate of said second P-type MOS transistor serves as a floating gate,
wherein said erasable programmable read only memory is capped by dielectric materials which are transparent to ultraviolet light.

[c7] 7.The erasable programmable read only memory of claim 6wherein said erasable programmable read only memory does not need to bias a certain voltage on a control gate for programming and thereby injecting hot carriers onto said floating gate.

[c8] 8.The erasable programmable read only memory of claim 6wherein during an erase mode, carriers stored in said floating gate are removed by exposing said floating gate to UV light irradiation and said UV light irradiates said floating gate through said dielectric materials capped on said erasable programmable read only memory.

[c9] 9.The erasable programmable read only memory of claim 6wherein said dielectric materials comprise any material that is UV-transparent.